ASCON

Submission to the CAESAR Competition

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DIAC 2016

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TU Graz

Our Team

- Christoph Dobraunig
- Maria Eichlseder
- Florian Mendel
- Martin Schläffer




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Main Design Goals

- Security
- Efficiency
- Lightweight
- Simplicity
- Online
- Single pass
- Scalability
- Side-Channel Robustness

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General Overview

- Nonce-based AE scheme
- Sponge inspired

	ASCON-128	ASCON-128a
Security	128 bits	128 bits
Rate (r)	64 bits	128 bits
Capacity (c)	256 bits	192 bits
State size (b)	320 bits	320 bits

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Working Principle

The encryption process is split into four phases:

- Initialization
- Associated Data Processing
- Plaintext Processing
- Finalization

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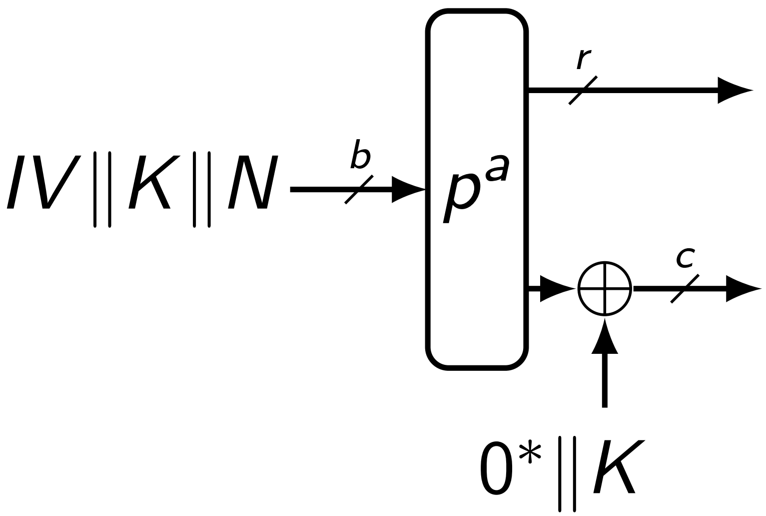
Initialization

- **Initialization:** updates the 320-bit state with the key K and nonce N



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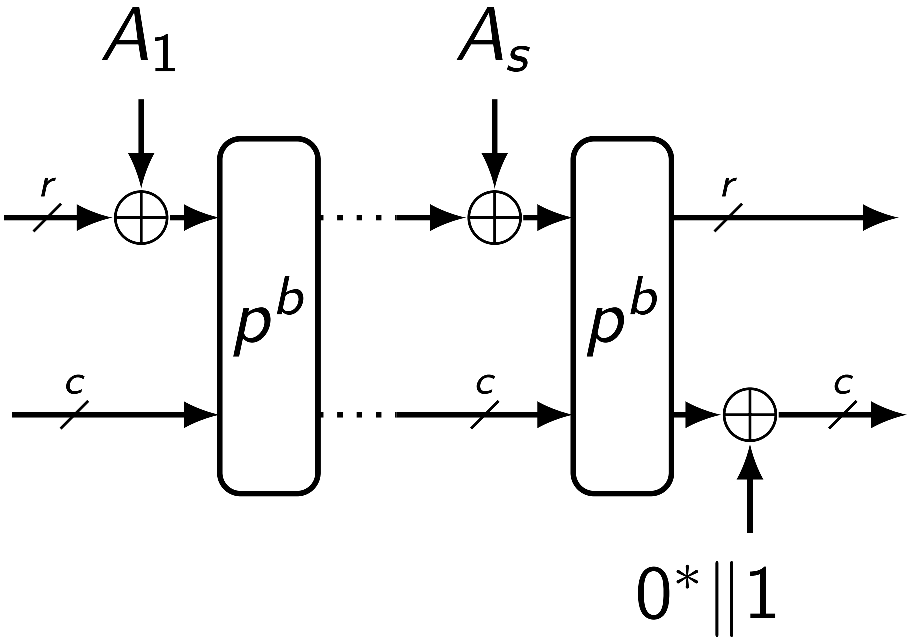
Associated Data

- **Associated Data Processing**: updating the 320-bit state with associated data blocks A_i



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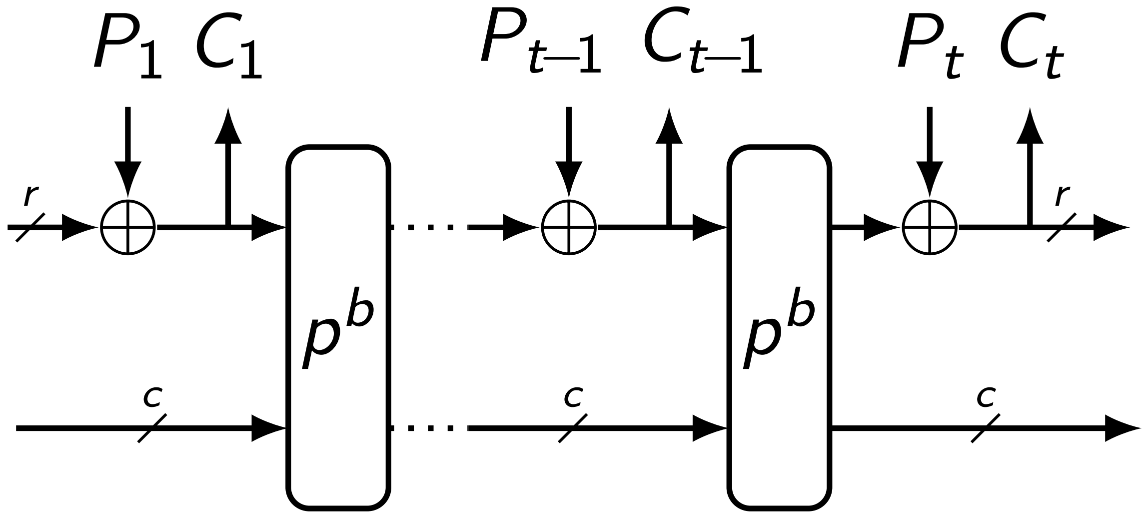
Encryption

- **Plaintext Processing**: inject plaintext blocks P_i in the state and extract ciphertext blocks C_i



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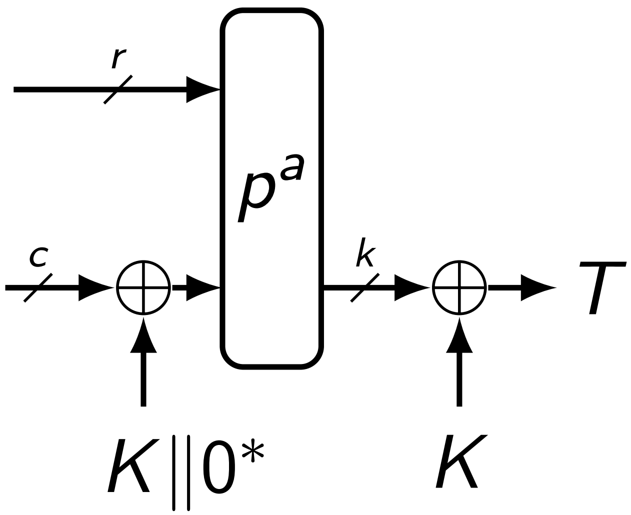
Finalization

- **Finalization:** inject the key K and extracts a tag T for authentication



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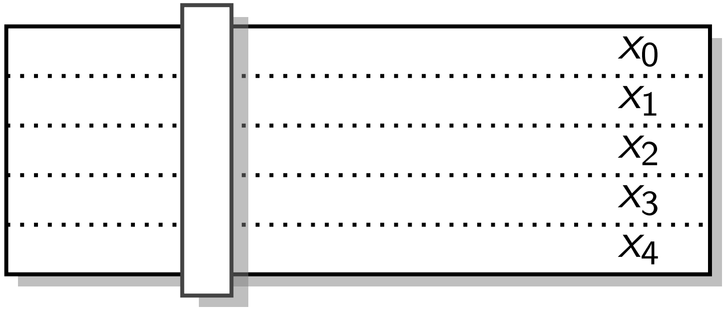
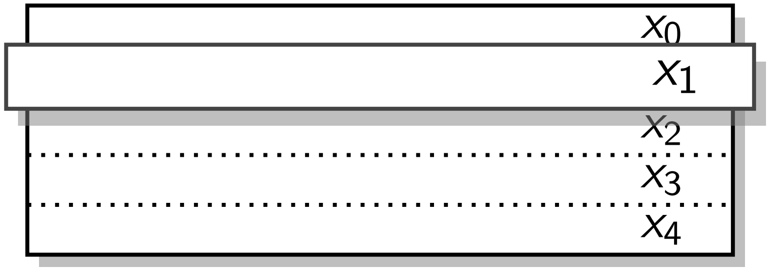
Permutation

- SP-Network:
  - S-Layer:



  - P-Layer:



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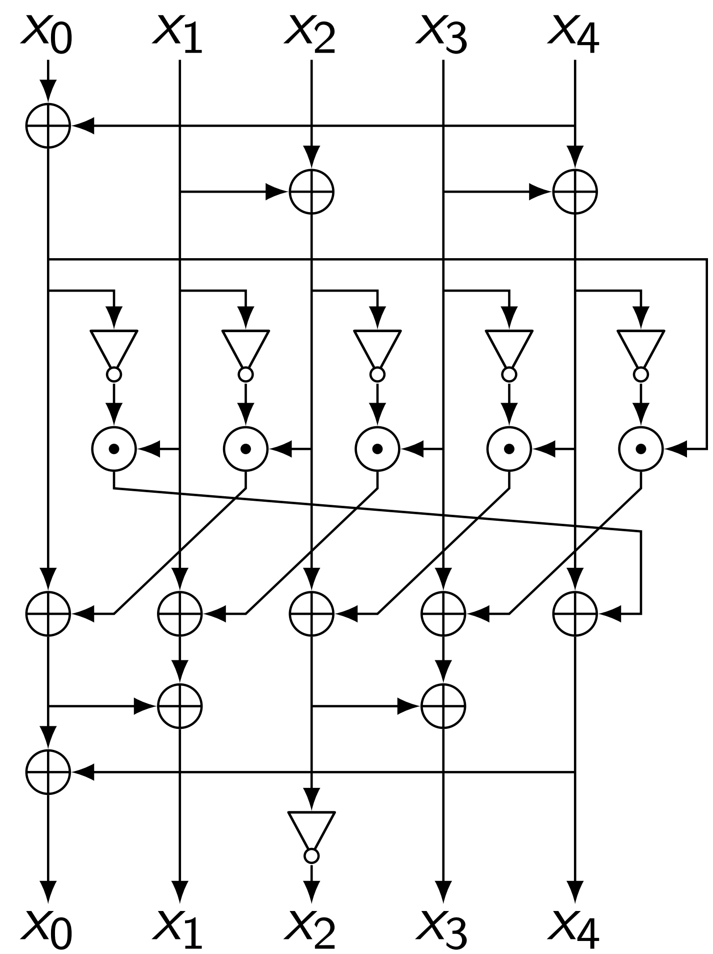
Permutation: S-Layer

- Algebraic Degree 2
  - Ease TI (3 shares)
- Branch Number 3
  - Good Diffusion
- Bit-sliced Impl.



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Permutation: P-Layer

- Branch Number 4

$$\Sigma_0(x_0) = x_0 \oplus (x_0 \ggg 19) \oplus (x_0 \ggg 28)$$
$$\Sigma_1(x_1) = x_1 \oplus (x_1 \ggg 61) \oplus (x_1 \ggg 39)$$
$$\Sigma_2(x_2) = x_2 \oplus (x_2 \ggg 1) \oplus (x_2 \ggg 6)$$
$$\Sigma_3(x_3) = x_3 \oplus (x_3 \ggg 10) \oplus (x_3 \ggg 17)$$
$$\Sigma_4(x_4) = x_4 \oplus (x_4 \ggg 7) \oplus (x_4 \ggg 41)$$

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Tweak for Round 3: Addition of Constants

- Modification of the round constant schedule
- Similar to FIPS 202
- Increase compatibility with other sponge modes
- No impact on existing security analysis

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Security Analysis

- Differential and Linear Cryptanalysis

Rounds	Differential	Linear
1	1	1
2	4	4
3	15	13
4	44	43
≥ 5	> 64	> 64

ASIACRYPT 2015

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Security Analysis

- Analysis of round-reduced versions

Method	Rounds	Complexity
cube-like	5/12	2^{35}
	6/12	2^{66}
differential-linear	4/12	2^{18}
	5/12	2^{36}

CT-RSA 2015

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Implementation/Performance

- Software
  - Intel Core2 Duo
  - ARM Cortex-A8

- Hardware
  - High-speed
  - Low-area

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Software Implementation

- Intel Core2 Duo

	64	512	1024	4096
ASCON-128 (cycles/byte)	22.0	15.9	15.6	**15.2**
ASCON-128a (cycles/byte)	17.7	11.0	10.5	**10.3**

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Software Implementation

- Intel Haswell (four message per core)

	64	**512**	**1024**	**4096**
ASCON-128 (cycles/byte)	10.5	7.3	7.1	**6.9**
ASCON-128a (cycles/byte)	8.5	5.3	5.0	**4.8**

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Hardware Implementation

- Unprotected Implementations

	Variant 1	Variant 2	Variant 3
Area **(kGE)**	7.1	24.9	**2.6**
Throughput **(Mbps)**	5 524	**13 218**	14

DSD 2015

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Hardware Implementation

- Threshold Implementations

	Variant 1	Variant 2	Variant 3
Area **(kGE)**	28.6	123.5	**7.9**
Throughput **(Mbps)**	3 774	**9 018**	14

DSD 2015

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Applications (Use Cases)

- Lightweight Applications
- High-Performance Applications
- Defense in Depth

Internet of Things

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Lightweight Applications

- Small hardware area
- Efficiency in hardware
- Natural side-channel protection
- Limited damage in misuse settings
- Low overhead for short messages

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High-Performance Applications

- Efficiency on modern CPUs
- Efficiency on dedicated hardware
- Natural side-channel protection

Thank you!

http://ascon.iaik.tugraz.at

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